Temperature Acceleration of Thin Gate-Oxide Degradation

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Abstract—The temperature dependence of $T_{BD}$ and $Q_{BD}$ of ultra-thin (3.9 nm thick) gate oxides was studied for $p^+$-poly Si PMOS and $n^+$-poly Si NMOS capacitors. It was observed that the temperature acceleration of $T_{BD}$ exhibits a non-Arrhenius behavior, meaning that no activation energy could be determined. Furthermore for $p^+$ gate devices both $T_{BD}$ and $Q_{BD}$ exhibit a stronger temperature dependence compared to $n^+$ poly-Si MOS devices. Also the dependence on the gate voltage is much stronger. This might have consequences for the reliability of $p^+$ gate devices under operating conditions.

Keywords — gate oxide

I. INTRODUCTION

Gate oxide reliability has always been one of the key problems in the down-scaling of CMOS devices [1,2,3]. As the oxide thickness is scaled down to a thickness of only a few nanometers additional reliability problems, like the strong temperature acceleration of gate oxide breakdown, severely limit the further downscaling of the oxide thickness [3]. Until now gate oxide reliability and temperature acceleration of time-to-breakdown ($T_{BD}$) of ultra-thin gate oxides was studied mainly for $n^+$ poly-Si gate devices [3,4]. Due to the increasing use of so-called double-flavored poly-Si processes the degradation of ultra-thin dielectrics using a $p^+$ poly-Si gate is also a major concern.

In this paper the temperature acceleration of time-to-breakdown for a $p^+$-poly-Si gate PMOS devices and $n^+$-poly-Si gate NMOS samples on 3.9 nm oxides is compared. It is found that for devices with a $p^+$-doped gate both $T_{BD}$ and $Q_{BD}$ (Charge-to-breakdown) exhibit a stronger temperature acceleration than devices with an $n^+$ doped gate. Also the $p^+$ gated devices show a stronger dependence on the dependence on gate voltage.

II. EXPERIMENTAL

A. Sample description

$p^+$ poly-Si PMOS (from now on PMOS) and $n^+$ poly-Si NMOS (from now on NMOS) capacitor structures and gated diodes were fabricated on 3.9 nm thick thermally grown gate-oxides. The area of the PMOS and NMOS capacitors was 50x50 $\mu$m² and 300x300 $\mu$m² respectively. Note that due to the difference in capacitor area the absolute values of the $T_{BD}$ and $Q_{BD}$ cannot be compared without taking an area scaling factor into account.

B. Measurement conditions

Constant voltage stressing (CVS) was used to determine the time-to-breakdown ($T_{BD}$) and charge-to-breakdown ($Q_{BD}$). As a trigger the first breakdown event was taken (soft breakdown, hard breakdown or increase in noise). The wafer temperature was varied between room temperature (25°C) and 200°C.

III. RESULTS AND DISCUSSION

Figure 1 and 2 show the current density of the gate-to-substrate- leakage as a function of the gate voltage measured on gated-diodes for PMOS and NMOS devices respectively. It is evident that the temperature dependence of the tunneling current is weak since tunneling itself is not dependent on the temperature. However the number of electrons at a given energy level does depend on the temperature as does the
tunneling barrier height. From figure 1, especially at negative gate bias, it can be seen that the PMOS leakage current shows a stronger temperature dependence just before breakdown. For both NMOS and PMOS this leads to lower breakdown voltage at elevated temperatures. It can also be noted that the NMOS devices (figure 2) show a larger asymmetry in onset of conduction compared to PMOS devices (figure 1). The difference in tunneling behavior has been discussed previously [5]. As a consequence of this asymmetry the current density of the NMOS device might differ as much as two orders of magnitude for both polarities under constant voltage stressing (CVS). Under constant current stressing (CCS) the absolute value of the voltage can differ by as much as one Volt. CVS has been proposed over CCS to evaluate gate oxide reliability [6]. Therefore in our study both $T_{BD}$ and $Q_{BD}$ are evaluated under CVS conditions.

Figures 3 and 4 show the $T_{BD}$ determined by CVS for PMOS and NMOS devices respectively as a function of the applied gate voltage at a 25, 100 and 200°C. The dotted lines are the mirrored fits for the negative bias data. Comparing figures 3 and 4 it is clear that the $T_{BD}$ results for PMOS devices show a considerable asymmetry with bias polarity and the NMOS devices show only a slight polarity gap.

DiMaria [7] has suggested that plotting the $T_{BD}$ as a function of the gate voltage would lead to near universal behavior (almost no asymmetry). Since for thin oxides the electrons tunnel almost ballistically through the oxide (loose no energy) the gate voltage approximately determines the injected electron energy with respect to the Fermi-level. So the gate voltage is the determining factor rather than the electric field as was the case for thicker oxides. Our PMOS data is not in accordance with this observation.

Figure 1: PMOS current density versus gate voltage for temperatures between 25 and 200°C.

Figure 2: NMOS Current density versus gate voltage for temperatures between 25 and 200°C.

Figure 3: $T_{BD}$ measurements for PMOS gate devices between 25 and 200 °C. Dotted lines are fit for negative $V_g$.

Figure 4: $T_{BD}$ measurements for NMOS gate devices between 25 and 200 °C. Dotted lines fit for negative $V_g$. 
Comparing the slopes of the curves in figures 3 and 4 gives a stronger dependence of $T_{BD}$ on the gate voltage $V_g$ under CVS for PMOS compared to NMOS. Nicollian et. al. have reported equal $V_g$ dependence of $T_{BD}$ for PMOS and NMOS devices under positive gate voltage stressing for devices with 2.7 nm oxide thickness [8]. Our data was taken for 3.9 nm gate oxides. The observed difference in $V_g$ dependence for the studied oxide thickness of 3.9 nm is not clear but might be due to a difference in tunneling mechanism or a difference in Fermi-level of the gate.

It is immediately clear from figures 3 and 4 that for both gate types and both voltage polarities the $T_{BD}$ depends strongly on the temperature. Note that due to the difference in gate-oxide area the absolute values of $T_{BD}$ for NMOS and PMOS capacitors cannot be compared.

In figure 5 the temperature dependence in $T_{BD}$ for both gate types taken at $V_g=\pm4.6$V is depicted. The linear dependence of $T_{BD}$ on the temperature indicates a typical non-Arrhenius behavior, which is consistent with previous publications [3,4] for n$^+$ poly-Si gate devices with thin gate oxides. From figure 5 it is obvious that the temperature dependence of $T_{BD}$ is significantly steeper for PMOS than for NMOS capacitors. For both gate types the dependence of $T_{BD}$ on the temperature is slightly stronger for gate injection ($V_g<0$). This could be due to minor structural differences in the two interfacial regions.

The observed strong temperature dependence of $T_{BD}$ as shown in figures 3, 4 and 5, cannot be explained by an increase in gate leakage current as can be seen from figures 1 and 2. A likely explanation for the decrease in $T_{BD}$ with temperature is an increase in the defect generation rate in combination with a decrease in total number of defect at breakdown [3]. The difference between PMOS and NMOS temperature dependence might be due to a difference in one of these two parameters.

Figure 6 depicts the total injected charge until breakdown, $Q_{BD}$ derived from $T_{BD}$ under CVS conditions for PMOS devices as a function of the stress voltage at 25, 100 and 200°C. Also the temperature dependence of NMOS $Q_{BD}$ at 25 and 200°C is shown for comparison. Plotting the data in this way three things are striking.

First the temperature dependence of $Q_{BD}$ is larger for PMOS compared to NMOS devices as was the case for $T_{BD}$. Secondly the polarity gap for PMOS capacitors in $Q_{BD}$ becomes very small, as was also observed by Nigam et.al. who have found a universal curve for $Q_{BD}$ versus $V_g$ for PMOS devices at both polarities and all process conditions [6]. For NMOS devices however we found a significant polarity gap in $Q_{BD}$. This is consistent with the observed symmetric $T_{BD}$ data (figure 4) and the asymmetry in the gate current (figure 2) for NMOS. For thinner gate oxides Nicollian et.al. [8] have shown that interface trap generation is the dominant mechanism for stress-induces-leakage-current (SILC) which determines $Q_{BD}$. However breakdown remains controlled by bulk trap generation and is voltage driven. The observed polarity gap in $Q_{BD}$ for NMOS and the absence of one for PMOS and the reverse effect in $T_{BD}$ (figures 3+4) might be an indication that a different breakdown mechanism is dominant.

Finally, for this oxide thickness the $Q_{BD}$ for PMOS capacitors depends strongly on the gate voltage, but the NMOS capacitors only show a weak dependence on the gate voltage.
IV. SUMMARY AND CONCLUSIONS

We have shown strong temperature dependence of gate oxide $T_{BD}$ and $Q_{BD}$ for PMOS devices using p$^+$-poly Si gates and NMOS devices with n$^+$-poly Si gates. The temperature dependence cannot be explained by the observed small increase in gate leakage current with increasing temperature.

The PMOS devices show a much stronger temperature dependence in both $T_{BD}$ and $Q_{BD}$ than the NMOS devices. The NMOS devices show almost no polarity gap in $T_{BD}$ with respect to bias polarity but show a strong gap $Q_{BD}$ results. For PMOS devices the polarity gap does exist in $T_{BD}$ but almost vanishes when $Q_{BD}$ is plotted. Although the origin of difference between PMOS and NMOS device reliability is not identified yet, a possible explanation might be the difference in injection mechanisms. At this moment we cannot rule out the possibility that for this gate oxide thickness a difference in breakdown mechanism plays a role.

The strong temperature dependence of the $T_{BD}$ and $Q_{BD}$ has drastic implications for the lifetime predictions of devices with increasing power dissipation (and hence operating temperature). Further work on different oxide thicknesses and stress conditions is necessary to gain more insight in the actual mechanisms to be able to make more accurate lifetime predictions.

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REFERENCES


