A 3-D Circuit Model to evaluate CDM performance of ICs

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Abstract

This paper presents a physical description of the static charge flow through an IC during a CDM event. Based on this description, an equivalent 3-D circuit to model the complete IC under CDM stress is proposed. The model takes into account various factors like package parasitics, substrate resistance, parasitic contacts of the circuit elements with the substrate, bus line resistances, distribution of protection devices. It allows studying the influence of these factors on the voltage transients seen across the gate-oxides of MOS transistors. CDM measurements on an IC with rail based protection showed gate-oxide failure at the MOS transistors in the internal core circuitry. The proposed circuit model is applied to study the voltage transients between the internal MOS transistors gate and local substrate during CDM stress and thereby explain the reason for the observed gate-oxide failure. It is found that the $V_{SS}$ line contact distribution with the substrate rail enhances CDM robustness, provided the power lines ($V_{SS}$ and $V_{DD}$ line) are well clamped to each other.

1. Introduction

The Charged Device Model (CDM) type of electrostatic discharge (ESD) occurs when a charged IC touches a grounded surface. Thus in this case, the IC is both the source and discharge path for the static charge. CDM stress results in voltage overshoots across the circuit elements. When the voltage drop across the gate-oxide of any MOS transistor exceeds its breakdown threshold voltage level, gate-oxide failure results. With continuous scaling down of device dimensions, especially thinning down of gate-oxides, the vulnerability to CDM gate-oxide failure has increased. For example in a 0.12 µm technology node where the gate-oxide thickness is 3 nm, the gate-oxide breakdown threshold voltage can be ~10 V for 1 ns stress time. The major block to hinder the development of a CDM robust design is the lack of knowledge on the source of discharge current and its path through the circuit during CDM stress. Measurement of internal voltage transients during CDM stress does not give useful information, as the parasitic effects of the additional test set-up would distort the fast transient signals significantly. Failure analysis apart from being very laborious only gives the information about the failure location. Circuit simulations on the other hand can help access the internal nodes. But the reliability of circuit simulation results depends on how accurately the circuit used in the simulation models the actual behavior of the IC during CDM stress. This paper studies the origin of the CDM discharge current and presents an equivalent circuit approach which can model the current and voltage transients across the entire IC during CDM stress. The circuit model is then applied to understand the cause for an
internal gate-oxide failure in an IC with rail based protection. This paper is organized as follows: In section 2, the origin of discharge current during CDM stress and the basic considerations for CDM circuit simulation is discussed. Section 3 explains how the full chip 3-D CDM circuit model is built. In section 4, the advantages of the proposed circuit model over the existing circuit models are detailed. CDM measurement result on an IC with rail based protection in 0.12\textmu m technology node is detailed in section 5. The circuit model presented is applied to the IC and the simulation results are used to investigate the reason for the observed gate-oxide failure. A possible method of reducing internal voltage transients is proposed in section 6. In the final section the results of the work are summarized.

2. Basic considerations for CDM circuit model

Charge on the IC package is capacitively coupled to the conducting layers within the IC as shown in figure 1. In other words, a charged IC is equivalent to several pre-charged capacitors. When any one of the IC pin touches a grounded surface, all these capacitors discharge through their connections to the grounded pin. The extent to which each of these capacitors influences the CDM performance of an IC depends on their magnitude and their discharge paths through the circuit. In this respect, the capacitance formed by the die attachment plate with the ground, \( C_{SUB} \) plays a significant role [1]. This is because of its large magnitude when compared to other capacitors and as its discharge path is distributed throughout the entire circuit through the common substrate. Hence the circuit model used to evaluate CDM performance of an IC should model \( C_{SUB} \) and its discharge path through the substrate [2]. The capacitance formed by the bus lines in the circuit is less than \( C_{SUB} \) and so is the amount of charge stored in them. However the contribution of these capacitors can change from one circuit design to another and the relative contribution of all these capacitors can change from one package type to another. The basic equivalent circuit that can best model an IC under CDM stress is shown in figure 1. The CDM current sources are modeled by pre-charged capacitors, substrate capacitance \( C_{SUB} \) and pin capacitance \( C_{PIN} \). The discharge of these capacitors through the grounded pin models the CDM discharge of the IC. The other IC capacitors formed by the metal layers in the circuit design with the ground are neglected in its first approximation. However their effect must be included when they are of significant magnitude. CDM discharge is modeled by the sudden switching of \( V_{SWITCH} \) from stress level say \( V_{CDM} \) to 0 V as shown in figure 1.

![Figure 1. IC chip under CDM test set-up along with its equivalent circuit model (Capacitors are pre-charged at \( V_{CDM} \)).](image1)

![Figure 2. Equivalent 3-D resistive network to model substrate resistance and capacitance.](image2)
3. Building of the full chip model

This section explains how the various parameters of an IC under CDM stress are modeled in the circuit simulation.

A. IC package: Package parameters play a significant role in determining the CDM withstand level of an IC, by being both the source and part of the discharge path for the CDM current. The capacitance associated with the IC package, mainly $C_{SUB}$, determines the amount of charge stored in an IC and the other package parasitics like inductance and resistance from the lead frame and bond wire affect the shape of the CDM discharge current waveform. These package parameters are determined from S-parameter measurements and are included in the model as shown in figure 1.

B. Substrate resistance and capacitance: The discharge path of $C_{SUB}$ consists of silicon substrate and the circuit elements which are directly (resistive) or indirectly (capacitive) connected to it. The substrate is divided into smaller unit volumes and each unit volume is modeled by a 3-D resistive network as shown in figure 2. One end of the network is connected to $C_{SUB}$ and the other end to the circuit elements in that volume.

C. Circuit Elements: Any circuit in general consists of protection devices, bus lines and internal core circuitry. Each unit volume is connected to the circuit elements in that respective volume. The behavior of the protection devices are modeled by the compact circuit model applicable to both normal and CDM operational conditions [3]. The compact model captures the bi-directional nature of the device in both positive and negative CDM stress. The parasitic bus line resistances of the power lines are taken into account. The circuit elements have direct resistive contact or indirect diode contact with the substrate. Figure 3 shows the equivalent CDM circuit model for a logic inverter used in the circuit simulation. This circuit representation holds good under the assumption that the IC is not powered up during CDM discharge.

The accuracy of the circuit model proposed depends on the grid size used. Hence it can be used to study voltage transients only in a small volume of the circuit during one simulation run.

4. Advantage of the 3-D circuit model over previously existing CDM circuit models

The full chip CDM circuit models presented earlier assumes the capacitance formed by the power lines $V_{DD}$ and $V_{SS}$ as CDM current sources [4],[5]. As a result the CDM simulation results cannot be used to perceive gate-oxide failures that can arise from voltage drop across the gate and substrate nodes of MOS transistor. The actual amount of CDM current conducted through the power lines depends largely on the type of contact they make with the substrate. The parasitic influence of the substrate on the CDM performance was considered for simulation by Etherton [6]. But the substrate was modeled by a 2-D resistive network and the CDM performance was evaluated by studying voltage transients across the gate and source nodes. As the discharge path is from the substrate to the circuit during CDM stress, grounding of a charged IC does not only cause voltage drop across the gate and source nodes of MOS transistor, but also across the gate and substrate nodes of MOS transistor. Accumulated charge on $C_{SUB}$ finds its way to any substrate connection in the circuit, possibly leading to potential drops along the surface of the substrate. Because of this the potential at the substrate node of MOS transistor can be quite different from that of its source node. As substrate also forms a major source of CDM current, the source and bulk (or substrate) nodes of the MOS transistors are not always at the same potential. Hence monitoring the potential drop across the gate and source nodes alone will be insufficient.

The 3-D nature of the circuit model takes into account all the parasitic contacts which the circuit elements like MOS transistors, resistors and power lines make with the substrate and thus helps monitor the voltage transients across the gate and substrate nodes of the internal MOS transistors.

5. CDM measurement results and discussions

An IC with rail based protection housed in CDIL40 pin package was subjected to CDM stress measurements. The
IC design is a ring of I/O cells in 0.12 µm technology node. Each I/O cell also includes some basic circuitry and the circuits are interconnected to other I/O cells.

Failure analysis showed gate-oxide failure at one of the first input inverters, whose gate is connected to the output of a core circuit at a completely different location. Figure 4 shows a portion of the IC design with the failure location. In a rail based protection, each I/O pad is clamped to the power rails via output drivers (parasitic diodes) and all the \( V_{DD} \) lines are clamped to their respective \( V_{SS} \) lines by BIGFETs. The protection circuit is designed in such a way that the CDM current from all power rails finds at least one forward biased diode path to the discharged pin and the power clamps across the power lines ensure that the voltage drop across the power lines are always clamped during the ESD stress. Thus if we look at power lines as the only CDM current sources, the voltage at the internal node will be at an intermediate value between the voltage levels at \( V_{DD} \) and \( V_{SS} \) lines during CDM stress and hence gate-oxide failure from voltage overshoot across gate and source nodes will be low. But we have shown \( C_{SUB} \) to be the main source of CDM current and that the discharge of \( C_{SUB} \) can cause large lateral substrate potential drops if the substrate is not frequently contacted to the \( V_{SS} \) lines, which can result in internal gate-oxide failure. Also, the voltage level at the internal nodes can be affected by its parasitic contacts which the node makes with the substrate. The 3-D circuit model takes into account these effects and helps investigate the internal voltage transients and study the cause for gate-oxide failure at this location.

6. Simulation results
A 3-D equivalent circuit of the IC is built as explained in section 2 and a CDM stress of -300 V is simulated on the complete IC (Case-A). The voltage drop across each substrate node with respect to the discharged pin at time

\[ t = t_{peak} \] during CDM discharge is shown in figure 5. \( t_{peak} \) is the time at which the current discharging through the circuit is maximum. The presence of P+ substrate contacts and protection devices closer to the I/O pads and no substrate contacts in the central region of the IC design, creates two extreme zones with regard to voltage transients during CDM stress. A first one, the safe zone where the substrate is closer to the potential drop across the protection device (\( V_{hold} \)) and a second one, the dangerous zone, where the voltage transients at the substrate nodes are much larger than \( V_{hold} \). The vulnerable circuits are in the region between these zones. In this paper we have limited our discussion to the study of the voltage transient across the gate-oxide of T3 alone. Figure 6 shows the voltage transients across the gate-oxide of T3 under -300 V CDM stress. From figure 6, we see that the voltage drop across the gate and substrate nodes of T3 is much larger than the voltage drop across its gate and source nodes. Under negative CDM stress, the output driver to the \( V_{DD} \) line acts as a forward biased diode and is fully conducting, while the output driver to the \( V_{SS} \) line is reverse biased. Therefore one would expect the CDM current from the substrate to discharge through the power clamp (BIGFET) into the ground through the output driver of the \( V_{DD} \) line. From figure 6 we see that the potential drop across the gate and source node initially rises but drops down later on. This should not happen if the CDM current from the substrate was discharged through the power clamp. The drop in the potential occurs when the voltage drop across the protection device (PD-1) to the substrate rail increases beyond its avalanche breakdown voltage, then
making the parasitic bipolar junction transistor of the output driver trigger on. As the P+ substrate contacts forms the lowest impedance discharge path, most of the CDM current is discharged directly via PD-1 instead of flowing through the power clamp. Also seen in the figure is that the gate potential of T3 goes below its source potential. The deviation of the gate potential from its intermediate value between the two power lines, depends on the difference in the amount of CDM current conducted through the two power lines and the parasitic influence of the substrate on the gate potential. The circuit design is slightly modified by locally shorting the VSS line to the P+ substrate contact at all the pin locations and simulation is repeated. For convenience we call the modified circuit design with additional substrate contacts as Case-B and the original circuit design as Case-A. The voltage drop across the gate-oxide of T3 with additional substrate contacts is shown in grey in figure 6. From figure 6 we see that with an increased number of substrate contacts to the VSS line, the voltage drop across the gate and substrate decreases while that of the gate and source increases. This observation is explainable as follows. By increasing the number of VSS line contacts with the substrate rail (Case-B), the potential at the substrate node of T3 is brought closer to its source potential and the amount of CDM current discharged through the VSS line is greatly increased. As the power lines are clamped, the voltage drop across the gate and source nodes will be kept below the clamping voltage across the power lines and hence the chance of gate-oxide failure would be greatly reduced. But as the amount of current conducted through the power lines VDD and VSS increases, their local potential can differ significantly depending on the amount of current conducted through it and the bus line resistance. Distribution of power clamps within the circuit will help clamp the voltage across the power lines effectively.

7. Conclusions

The major source of CDM current is from C_{SUB} and its discharge path is through the substrate contact into the circuit. CDM discharge causes large voltage transients between both the gate and source nodes and between the gate and substrate nodes. Protection circuits are designed assuming the power lines to be the only path of CDM discharge current. This is not true. There are several discharge paths for the CDM current from the substrate to other circuit elements. By increasing the number of direct substrate contacts with the power lines, more of the CDM current will be directed into the power lines. Only then the protection circuits become effective. By increasing the discharge current flow through the power lines, the local potential drop across these power lines can vary quite significantly depending on the amount of current conducted through them and its bus line resistance. To reduce such differences in the local potential, power clamps must be distributed within the circuit.

Reference